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Wafer level packaging technology for silicon resonators

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Abstract

Recently, a family of low frequency silicon resonators with AlN piezoelectric activation has been developed. These devices need to be operated under vacuum. The main motivation for the packaging of resonator under vacuum is to increase the Q factor, and to guarantee the long-term stability of the resonance frequency. In order to minimize the size of packaged resonators, wafer level packaging (WLP) has been chosen.

Keywords: Silicon resonator; AlN; packaging; anodic bonding; Au-Sn sealing

1. Introduction

Electronic devices of all kinds need timing references. Currently, the main technology for clock products is quartz. Miniaturization of quartz has been driven by the mobile phone industry. Today 32kHz quartz resonator are found in packages as small as 2x1.25x0.6mm^3 (Epson Toyocom FC-12M) while 30MHz or above resonators can be found in 1.6x1.25x0.3mm^3 packages (TEW Tokyo DenpaTAS1612C/D). Since the early 1980s, companies have been trying to replace quartz with silicon MEMS-based oscillators. Until recently however, the low temperature stability of silicon and the need for expensive ceramic or metal vacuum packaging prevented MEMS from becoming a serious alternative to quartz. SiTime claims the smallest integrated silicon resonator with electrostatic actuation packaged at the wafer level. The resonator cavity is sealed at high temperature (1000°C) and under high vacuum during the processing of the resonator itself (not a backend post-processing)[1]. An alternative – piezoelectric through AlN - actuation solution has been proposed in recent years [2, 3]. Devices covering a large frequency range from 20kHz to 36MHz were demonstrated. One of the major advantages of piezoelectric devices over electrostatic devices is that the impedance levels are much closer to those achievable with quartz and would hence allow similar drive circuits to be used.

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Low-cost, simple, reproducible, stable hermetic vacuum packaging technologies are required for many micro-devices such as inertial sensors, micromirrors and micromechanical resonators used in RF applications. Primary source of energy dissipation in micromechanical oscillators is air damping. Fig. 1 shows a plot of Q factor versus pressure for an extensional AlN/Si resonator operating at 1MHz. For this resonator, we can see that the Q is pressure limited above a pressure of approximately 1 mbar. In order to obtain stable values of Q factors higher than 100000, it is mandatory to maintain the resonator at a pressure below 1 mbar. Below 1 mbar, the dissipation associated with air damping becomes negligible compared to other loss mechanisms (clamping, thermoelastic damping, surface losses etc.). Typical packaging in metal or ceramic cans results in a larger size of components. In order to be competitive in terms of size with the quartz components available on the market, a high quality vacuum sealing process needs to be adapted for Si resonators. Vacuum packaging of devices has been investigated using a number of approaches including thin film encapsulation, anodic bonding, glass frit bonding and various solder bonding techniques. Thin film encapsulation and anodic bonding are proven and effective sealing techniques, in which pressures ranging from 10^{-3} mbar to 1 mbar have been demonstrated, but are limited to specified process conditions (material compatibility, thermal budget, planarity). Bonding techniques such as glass frit bonding and solder bonding, on the other hand, are particularly attractive because the glass frit or solder is melted during the bonding process allowing for bonds to non-planar surfaces. Getters are sometimes used to control pressure inside the cavity and reduce the effect of any outgassing that occurs from the sealing and device materials [4]. In this paper solutions for full WLP of the resonator have been demonstrated combining anodic bonding and AuSn sealing.

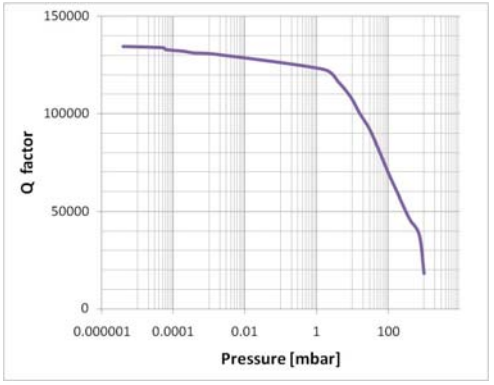

Figure 1: Q factor as function of pressure for 1 MHz extensional resonator.

2. Experimental and results

The generic technology proposed hereafter for packaging AlN/Si resonators consists in building a hermetic cavity around the resonator. This is done in three steps (Fig.2):

1. Fabrication of the AlN/Si resonator
2. Wafer-to-Wafer rear side packaging
3. Die-to-die front-side packaging performed under vacuum.

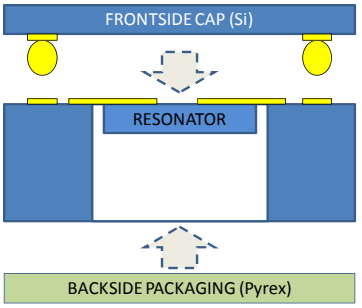

Fig. 2: Schematic view of packaging principle for AlN/Si resonators.

2.1. Fabrication of AlN/Si resonator

All types of resonators are built from (100)-oriented Silicon on Insulator substrates. the vibrating structure consists mainly of single crystal silicon that is oxidized on both sides (top and buried oxide), and that is topped by AlN and its electrodes. Polycrystalline piezoelectric (002) AlN films are deposited by magnetron sputtering on Pt (111) forming a piezoelectric activation for the SOI structure. All thin films are patterned by standard photolithography and dry etching. The Si beams are created by deep reactive ion etching (DRIE) of the Si device layer from the top side, followed by the DRIE of the Si handle from the backside. Fig.3 shows a top view of 1MHz extensional and 100kHz flexural AlN/Si resonators with sealing rings.

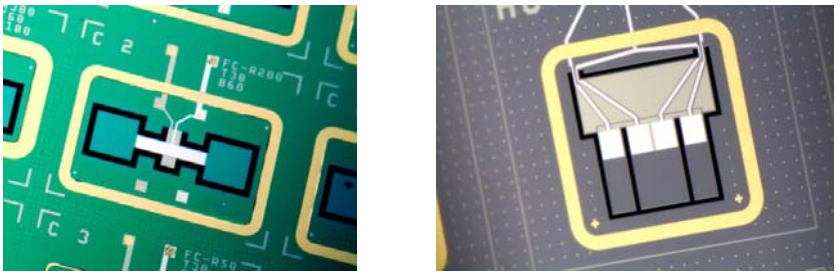

Fig. 3: Top view of 1MHz extensional (a) and 100kHz flexural (b) AlN/Si resonators with sealing rings

2.2. Wafer-to-Wafer rear-side packaging

The solution uses a capping Pyrex wafer sealed by anodic bonding. This bonding method requires an extremely smooth and residue free surface of the wafer. The thickness of silicon oxide on rear side of the wafer shall not exceed 500 nm. The bonding process is conducted at 350°C, -1200V, 3 mbar during 30 min. The performances of resonators were not altered during this sealing process. Thin (300 microns) Pyrex substrates have been hermetically bonded with device SOI wafers (thickness 100+390 microns).

2.3. Frontside packaging

Metallic alloy materials can provide very low permeability sealing characteristics. The resonator/Pyrex chips (Die-to-Die solution) are vacuum encapsulated using silicon caps and AuSn soldering technology for frontside capping. An under bump metallization (UBM) layer is deposited prior to sealing on the capping wafer. We use here a Ti:W(N) 200nm/Au 200 nm with a Au 2 µm socket. Galvanic AuSn ring is deposited with 5 micron of Sn and 10 micron of Au. A second UBM layer (TiW/Au) is deposited as well on the resonator during the processing. Fig.4a shows a view of a Si cap and its sealing ring before sealing.

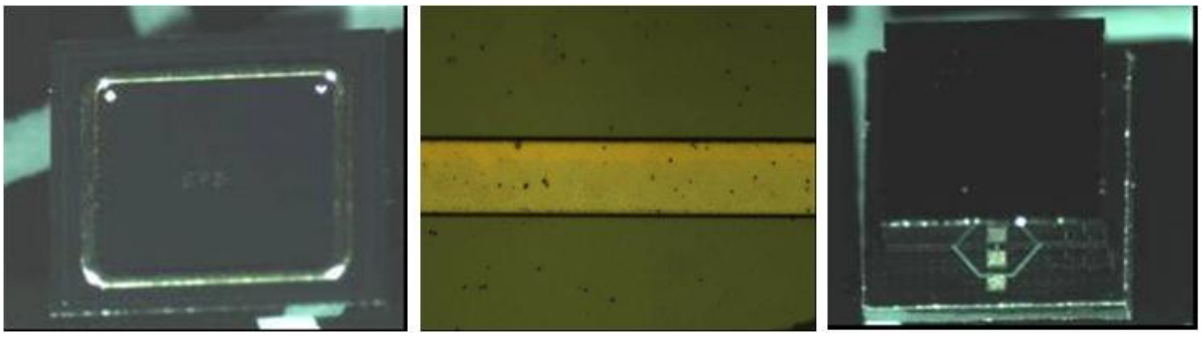

Fig. 4: (a) view of a Si cap and its sealing ring. (b) cross section view after sealing (UBM/Au/AuSn/UBM). (c) top view of 100 kHz packaged resonator

A reflow process was developed minimizing the size and amount of voids (thought to be Kirkendall voids), controlling the dendrite height and the amount of eutectic formed. The reflow process developed involves oxide reduction, annealing and AuSn (80/20) eutectic formation steps. A tacking process is involved before the vacuum sealing process to use the advantage of accurate alignment possible in a flipchip machine. Tacking is done using a tacking media which can be evaporated and degassed before the vacuum sealing step. The vacuum sealing is done at a peak temperature of 320ºC and the process time is optimized to have less consumption of the UBM. Pressure is needed during the sealing process to have uniform wetting throughout the ring due to the high surface tension of the AuSn eutectic. Fig.4b shows a cross section view after sealing process (UBM/Au/AuSn/UBM). In this version, the electrical contact with the resonator is established via metal lines crossing the sealing ring (Fig4c). The electrical signal and metal sealing ring are isolated by a passivation SiON layer.

2.4. Packaged resonators

1 MHz extensional mode resonators have been packaged using thin (200 μm) Si capping and Pyrex wafers (300 μm). The total size of the packaged resonator is 4x3x1 mm^3. The quality of vacuum in the cavity, and hence of the sealing, is monitored through measurements of the resonators Q factor. Packaged resonators exhibit a Q factor in vacuum as high as 140000. Resonators used in an oscillator with a dedicated circuit are still functional after 6 months, which shows that this packaging scheme is adapted to produce vacuum-tight cavities.
By using the same technology 100 kHz flexural resonators can be packaged. Further miniaturization can be obtained by integrating these resonators on buried cavities (hermetic cavities formed in SOI substrates). In this case, the backside sealing with Pyrex is avoided and the size of the single die yields 3x2.5x0.6 mm^3.

3. Conclusion

In this paper we presented a method for packaging AlN/SOI silicon resonators under vacuum.
Vacuum-tight packaged resonators have been fabricated by the following techniques:

- Backside packaging: anodic bonding with thin Pyrex wafer,
- Frontside packaging: Au-Sn eutectic sealing with capping silicon wafer.

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